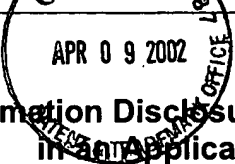


PTO-1449  <b>Information Disclosure Citation in an Application</b>		Application No. 09/918,295  Docket Number 068167.0108		Applicant(s) Traut, et al.  Group Art Unit 2181  Filing Date 7/30/01		
<b>U.S. PATENT DOCUMENTS</b>						
	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
A	5278973	1/11/94	O'Brien et al.	395	500	6/27/91
B	5301277	4/5/94	Kanai	709	301	12/23/91
C	5367628	11/22/94	Ote et al.	345	501	10/15/92
D	5448264	9/5/95	Pinedo et al.	345	508	6/14/93
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F	5502809	3/26/96	Takano	345	509	9/6/94
G	5640562	6/17/97	Wold et al.	395	652	2/27/95
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M	5831607	11/3/98	Brooks	345	333	1/25/96
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<b>FOREIGN PATENT DOCUMENTS</b>						
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
						YES NO
<b>NON-PATENT DOCUMENTS</b>						
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S	"Processor Instruction Sets," The PC Guide, version date 12/18/00, <a href="http://www.pcguide.com/ref/cpu/arch/int/inst-c.html">http://www.pcguide.com/ref/cpu/arch/int/inst-c.html</a> .					
T	"M68060 User's Manual," Motorola, 1994, pp. i-xviii; Section 4, Memory Management Unit, pp. 4-1 to 4-30, <a href="http://e-www.motorola.com/brdata/PDFDB/MICROPROCESSORS/32_BIT/68K-COLDFIRE/M680X0/MC68060UM.pdf">http://e-www.motorola.com/brdata/PDFDB/MICROPROCESSORS/32_BIT/68K-COLDFIRE/M680X0/MC68060UM.pdf</a> .					
U	"MPC750, RISC Microprocessor User's Manual," Motorola, 8/97, Contents, pp. iii-xvi; Chapter 5, Memory Management, pp. 5-1 to 5-34; Glossary, pp. Glossary-1 to Glossary-13, <a href="http://e-www.motorola.com/brdata/PDFDB/MICROPROCESSORS/32_BIT/POWERPC/MPC7XX/MPC750UM.pdf">http://e-www.motorola.com/brdata/PDFDB/MICROPROCESSORS/32_BIT/POWERPC/MPC7XX/MPC750UM.pdf</a> .					
EXAMINER				DATE CONSIDERED		
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PTO-1449				Application No. 09/918,295		Applicant(s) Traut et al	
<b>Information Disclosure Citation in an Application</b>				Docket Number 0681,67.0108		Group Art Unit 2181	
						Filing Date 07/30/2001	
<b>U.S. PATENT DOCUMENTS</b>							
		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
<b>FOREIGN PATENT DOCUMENTS</b>							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
<b>NON-PATENT DOCUMENTS</b>							
		<b>DOCUMENT (Including Author, Title, Source, and Pertinent Pages)</b>					
	A	U.S. Patent Application Serial No. 09/617,709, "System and Method for Emulating the Operation of a Translation Look-Aside Buffer", Traut, filed July 17, 2000					
	B	U.S. Patent Application Serial No. 09/617,669, "System and Method for Displaying Current Images of Virtual Machine Environments", Traut, et al., filed July 17, 2000					
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	D	U.S. Patent Application Serial No. 09/747,492, "System and Method for the Logical Substitution of Processor Control in an Emulated Computing Environment", Traut, filed December 21, 2000					
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Jean R. Homere					12/23/03		
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<b>PTO-1449</b>  <b>Information Disclosure Citation in an Application</b>				Application No. 09/918,295		Applicant(s) Traut, et al.	
				Docket Number 068167.0108		Group Art Unit 2181	
<b>U.S. PATENT DOCUMENTS</b>							
		<b>DOCUMENT NO.</b>	<b>DATE</b>	<b>NAME</b>	<b>CLASS</b>	<b>SUBCLASS</b>	<b>FILING DATE</b>
JRH	A	5,815,686	9/29/98	Earl, et al.	395	500	9/12/96
JRH	B	4,779,188	10/18/88	Gum et al.	364	200	10/19/87
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		<b>DOCUMENT NO.</b>	<b>DATE</b>	<b>COUNTRY</b>	<b>CLASS</b>	<b>SUBCLASS</b>	<b>TRANSLATION</b>
	C	EP 0 645 701 A2	26/09/94	EPO	G06F	9/455	YES X NO
<b>NON-PATENT DOCUMENTS</b>							
		<b>DOCUMENT (Including Author, Title, Source, and Pertinent Pages)</b>					
JRH	D	PCT International Search Report in International Application No. PCT/US 01/22276, International filing date 16/07/01, mail date 07/03/02.					
	E	Traut E, "Building the Virtual PC," Byte, McGraw-Hill Inc., Vol. 22, No. 11, pp. 51-52, 1 November 1997.					
	F	"Intel386 DX Microprocessor," Intel, pp. 32-58, 31 December 1995.					
	G	"Macintosh and Technology: Changing Chips in the Middle of the Stream, or Apple Takes a Risc," URL:www.btech.co/changingchips.html, paragraphs '0006!'-'0007!', retrieved 12/10/01.					
	H	"M68040 User's Manual," Motorola, Inc., Chapter 3, copyright 1990, revised 1992, 1993.					
	I	Osisek DL et al., "ESA/390 Interpretive-Execution Architecture, Foundation for VM/ESA," IBM Systems Journal, Vol. 30, No. 1, pp. 34-51, 1991.					
	J	Shang Rong Tsai et al., "On the Architectural Support for Logical Machine Systems," Microprocessing and Microprogramming, Vol. 22, No. 2, pp. 81-96, February 1988.					
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